CLAIMS

1. A circuit configured to interface with an etch tool, said circuit comprising:

an ESC input for receiving a first signal from said etch tool, said first signal indicating a magnitude of a chuck current passing through a chuck holding a wafer in said etch tool;

a VRF input for receiving a second signal from said etch tool, said second signal indicating a magnitude of a voltage difference between a plasma and said chuck in said etch tool;

an arc detect output indicating whether an arc event has occurred.

2. The circuit of claim 1 wherein said circuit is configured to prevent said arc detect output from indicating an occurrence of a chucking spike and a de-chucking spike in said etch tool.

3. The circuit of claim 1 wherein said first signal indicates an occurrence of the group consisting of a chucking spike, a de-chucking spike, and said arc event in said etch tool.

4. The circuit of claim 1 further comprising an ESC signal level detector connected to said ESC input, said ESC signal level detector being configured to provide an output when said first signal indicates an occurrence of the group consisting of a chucking spike, a de-chucking spike, and said arc event.

5. The circuit of claim 1 further comprising a VRF signal level detector connected to said VRF input, said VRF signal level detector being configured to provide an output when said second signal indicates that said plasma is activated.

6. The circuit of claim 1 further comprising a first gate having a first gate input, a second gate input, and a first gate output, said first gate input being connected to said ESC input and said second gate input being connected to said VRF input, said first gate being configured to output a third signal at said first gate output when said first signal indicates an occurrence of a de-chucking spike and said arc event and not output said third signal at said first gate output when said first signal indicates an occurrence of a chucking spike.

7. The circuit of claim 6 further comprising a power-on delay connected between said VRF input and said second gate input, said power-on delay being configured to prevent said first gate from outputting said third signal during said occurrence of said chucking spike.

8. The circuit of claim 6 further comprising a second gate having a third gate input, a fourth gate input, and a second gate output, said third gate input being connected to said first gate output and said fourth gate input being connected to said VRF input, said second gate being configured to output a fourth signal at said second gate output during

said occurrence of said arc event and not output said fourth signal at said second gate output during said occurrence of said de-chucking spike.

9. The circuit of claim 1 further comprising a storage module having an input and an output, said output of said storage module being connected to said arc detect output, said storage module being configured to store a third signal received at said input of said storage module and output said third signal at said output of said storage module, said third signal indicating an occurrence of said arc event.

10. The circuit of claim 6 further comprising a power-off advance connected to said first gate output, said power-off advance being configured to prevent said arc detect output from indicating said occurrence of said de-chucking spike.

11. A circuit configured to interface with an etch tool, said circuit comprising:

an ESC input for receiving a first signal from said etch tool, said first signal indicating a magnitude of a chuck current passing through a chuck holding a wafer in said etch tool;

a VRF input for receiving a second signal from said etch tool, said second signal indicating a magnitude of a voltage difference between a plasma and said chuck in said etch tool;

an arc detect output indicating whether an arc event has occurred;

wherein said circuit is configured to prevent said arc detect output from indicating

an occurrence of a chucking spike and a de-chucking spike in said etch tool.

12. The circuit of claim 11 wherein said first signal indicates an occurrence of the group consisting of said chucking spike, said de-chucking spike, and said arc event in said etch tool.

13. The circuit of claim 11 further comprising an ESC signal level detector connected to said ESC input, said ESC signal level detector being configured to output a third signal when said first signal indicates an occurrence of the group consisting of said chucking spike, said de-chucking spike, and said arc event.

14. The circuit of claim 13 further comprising a gate having a first gate input, a second gate input, and a gate output, said first gate input being connected to said ESC signal level detector and said second gate input being connected to said VRF input, said gate being configured to output a fourth signal at said gate output when said third signal indicates an occurrence of said de-chucking spike and said arc event and not output said fourth signal when said third signal indicates an occurrence of said chucking spike.

15. The circuit of claim 11 further comprising a VRF signal level detector connected to said VRF input, said VRF signal level detector being configured to output a third signal when said second signal indicates that said plasma is activated.

16. The circuit of claim 15 further comprising a gate having a first gate input, a second gate input, and a gate output, said first gate input being connected to said ESC input and said second gate input receiving said third signal, said gate being configured to output a fourth signal at said gate output when said first signal indicates an occurrence of said de-chucking spike and said arc event and not output said fourth signal when said first signal indicates an occurrence of said chucking spike.

17. The circuit of claim 11 further comprising a first gate having a first gate input, a second gate input, and a first gate output, said first gate input being connected to said ESC input and said second gate input being connected to said VRF input, said first gate being configured to output a third signal at said first gate output when said first signal indicates an occurrence of said de-chucking spike and said arc event and not output said third signal at said first gate output when said first signal indicates an occurrence of said chucking spike.

18. The circuit of claim 17 further comprising a power-on delay coupled between said VRF input and said second gate input, said power-on delay being configured to prevent said first gate from outputting said third signal at said first gate output during said occurrence of said chucking spike.

19. The circuit of claim 17 further comprising a second gate having a third gate input, a fourth gate input, and a second gate output, said third gate input being connected

to said first gate output and said fourth gate input being connected to said VRF input, said second gate being configured to receive said third signal outputted by said first gate and output a fourth signal at said second gate output during said occurrence of said arc event and not output said fourth signal at said second gate output during said occurrence of said de-chucking spike.

20. The circuit of claim 17 further comprising a power-off advance connected to said first gate output, said power-off advance being configured to prevent said arc detect output from indicating said occurrence of said de-chucking spike.